Form 3.54 Division-continuation
program application transmittal form
37 C.F.R. 1.53(b)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Docket No. HIT 2 010-1-1

Prior application: 07/344,455
Examiner: R. Harrell
Art Unit: 2315

The Assistant Commissioner for Patents
Washington, D.C. 20231
Box Patent Application

Sir:

This is a request for filing a continuation application under 37 C.F.R. 1.53(b), of pending prior application **U.S. Serial No. 07/344,455 filed on April 27, 1989 of Naoki Mitsuishi, which is a file wrapper continuing application of U.S. Serial No. 07/029,750 filed March 24, 1987 of Naoki Mitsuishi, now abandoned.**

For: **AN IC CARD HAVING A DEDICATED WRITE CONTROLLER FOR WRITING TO INCORPORATED EEPROM ON THE CARD (As Amended)**

1. XXX Enclosed is a complete copy of the prior application, including the oath or declaration as originally filed.

2. XXX A PRELIMINARY AMENDMENT is enclosed.

3. XXX A Request for Drawing Changes is enclosed.

4. XXX The filing fee is calculated below.

CLAIMS AS FILED IN THE PRIOR APPLICATION LESS ANY CLAIMS CANCELED BY PRELIMINARY AMENDMENT			
Basic Filing Fee (Large Entity)			$ 760.00
		No. of Extra Claims Present	Additional Rate
Total Claims	3	0	$ 0.00
Indep. Claims	1	0	$ 0.00

Total fee $ 760.00

5. XXX A check in the amount of $ 760.00 is enclosed.

6. XXX The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Account No. 06-0308.

CERTIFICATE OF EXPRESS MAIL

I hereby certify that this **TRANSMITTAL LETTER, CONTINUATION APPLICATION AND FILING FEE** are being deposited with the United States Postal Service by Express Mail Procedure in an envelope addressed to: Assistant Commissioner for Patents, Box Patent Application, Washington, D.C. 20231 on the 29 day of January 1999. **Express Mailing Label No. EL278351787US.**

P Stepka

Pamela Stepka

7. xxx An Information Disclosure Statement and the required form PTO-1449 are enclosed.

8. xxx Priority of application serial no. 61-65739, filed on March 26, 1986 in Japan is claimed under 35 U.S.C. §119. The certified copy has been filed (on May 21, 1987) in prior application U.S. Serial No. 07/029,750 filed March 24, 1987 of Naoki Mitsuishi, now abandoned.

9. xxx The power of attorney in the prior application is to Patrick R. Roche, Reg. No. 29,580. A copy of the power in the prior applications is enclosed. Also enclosed is a copy of an associate power of attorney to Mark S. Svat, Reg. No. 34,261, and Joseph D. Dreher, Reg. No. 37,123, filed in U.S. Serial No. 07/344,455. Please address all future communications to

Mark S. Svat
FAY, SHARPE, BEALL, FAGAN,
MINNICH & McKEE
1100 Superior Avenue, 7th Floor
Cleveland, Ohio 44114-2518
(216) 861-5582

I hereby verify that the attached papers are a true copy of prior application U.S. Serial No. 07/344,455 filed on April 27, 1989 of Naoki Mitsuishi which is a file wrapper continuing application of U.S. Serial No. 07/029,750 filed March 24, 1987 of Naoki Mitsuishi, now abandoned.

The undersigned declares further that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

January 29, 1999
Date

Joseph D. Dreher
Joseph D. Dreher
Reg. No. 37,123
Attorney of Record

Address of Signator:

FAY, SHARPE, BEALL, FAGAN,
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Naoki Mitsuishi

For : **IC CARD HAVING A DEDICATED WRITE CONTROLLER FOR WRITING TO AN INCORPORATED EEPROM ON THE CARD (as amended)**

Serial No. : 07/344,455

Filed : April 27, 1989

Attorney Docket No. : HIT 2 010-1

Assistant Commissioner For Patents
Washington, D.C. 20231

NOTIFICATION OF FILING OF CONTINUING OR DIVISIONAL APPLICATION

Dear Sir:

Notification is hereby being made of the filing of a:

- [X] continuation
- [ ] continuation-in-part
- [ ] divisional

application for this case

- [X] concurrently herewith
- [ ] on _____ *(date)*

Respectfully submitted,

Joseph D. Dreher
Reg. No. 37,123

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Pamela Stepka

"Express Mail" Mailing Label Number: EL278351787US

Date of Deposit: January 21, 1999

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By: Pamela Stepka

PATENTS ONLY

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF	:	Naoki Mitsuishi
FOR	:	**AN IC CARD HAVING A DEDICATED WRITE CONTROLLER FOR WRITING TO INCORPORATED EEPROM ON THE CARD (As Amended)**
SERIAL NO.	:	Unknown
FILED	:	Herewith
ATTORNEY DOCKET NO.	:	HIT 2 010-1-1

Cleveland, Ohio 44114-2518
January 28, 1999

PRELIMINARY AMENDMENT

Assistant Commissioner
for Patents
Washington, DC 20231

Dear Sir:

Please amend the above-identified application in the following manner before the examination thereof:

IN THE TITLE:

Please amend the title to read: AN IC CARD HAVING A DEDICATED WRITE CONTROLLER FOR WRITING TO INCORPORATED EEPROM ON THE CARD.

IN THE ABSTRACT OF THE DISCLOSURE:

Please add the following abstract:

ABSTRACT OF THE DISCLOSURE

A single chip type microcomputer includes at least a central processing unit (CPU), a random-access memory (RAM), a mask read-only memory (CPU) and an electrically writable ROM such as an electrically erasable and programmable read-only memory (EEP-ROM). The electrically writable ROM stores both the user program and data to be preserved. The microcomputer includes further a memory for storing a write control program for controlling the write operation to the writable ROM, and the electrically writable ROM and the memory are disposed at mutually different address positions on the address space of CPU. The proportion of size of the user program region and the data region in the writable ROM can be selected in a free proportion.

IN THE SPECIFICATION:

At page 1, as the first sentence following the title, please insert --This application is a continuation of U.S. Serial No. 07/344,455 filed on April 27, 1989 (pending) of Naoki Mitsuishi which is a file wrapper continuing application of U.S. Serial No. 07/029,750 filed March 24, 1987 of Naoki Mitsuishi (now abandoned);

Page 5, line 22, change "microcomputer" to --microcomputer--;

Page 6, line 4, change "write control circuit 7" to --write control unit 7 (Fig. 2)--;

line 28, delete "EEP-ROM";

Page 9, line 27, change "EEP-ROM 3" to --EEP-PROM 4--;

line 28, change "communcation" to --communication--;

Page 11, after line 28, add -- See discussion on Fig. 5, above.--

IN THE CLAIMS:

Please cancel claims 1 - 20.

Please add the following new claims 21 - 23.

21. A microcomputer comprising:

an electrically programmable ROM which has a first region to store a user program therein and a second region to store data therein;

a memory which stores a write control program for a writing to the electrically programmable ROM; and

a CPU which executes the user program and the write control program,

wherein the electrically programmable ROM and the memory are disposed at mutually different address positions,

wherein the user program includes a first instruction which changes a process of the CPU executing the user program to a process that controls a writing of the electrically programmable ROM based on the write control program stored in the memory, and

wherein the write control program includes a second instruction which returns the CPU to the process based on the executing of the user program stored in the electrically programmable ROM after completion of the process that controls the writing of the electrically programmable ROM.

22. A microcomputer according to claim 21,

wherein the memory which stores a write control program is a mask ROM.

23. A microcomputer according to claim 21,

wherein the memory which stores a write control program is a RAM that receives the write control program from the electrically programmable ROM.

REMARKS

The foregoing amendments are being submitted to place the subject application in better condition for examination. It is believed that no new matter has been added to this application. Early favorable action is hereby respectfully requested.

In addition to the foregoing, the applicant has supplied herewith a Request for Drawing Changes, the particulars of which are found therein.

Last, the Examiner is hereby apprised that the parent application, U.S. Serial No. 07/344,455 (filed April 27, 1989), is still pending as of the date of the filing hereof. A Hearing on the appeal in the parent case is scheduled for February 12, 1999.

Respectfully submitted,

FAY, SHARPE, BEALL, FAGAN,
MINNICH & McKEE

January 29, 1999
Date

Joseph D. Dreher
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor: Naoki MITSUISHI

Invention: Microcomputer

SPECIFICATION

To All Whom It May Concern:

Be it known that I, Naoki MITSUISHI, a citizen of Japan, residing at Kodaira-shi, Tokyo, Japan having invented certain new and useful improvements in:

MICROCOMPUTER

of which the following is a specification.

MICROCOMPUTER

BACKGROUND OF THE INVENTION

This invention relates generally to microcomputer technique, and more particularly to techniques which are effective when applied to a single chip type microcomputers with a built-in electrically writable ROM, such as an EEP-ROM (Electrically Erasable and Programmable Read-Only Memory). For instance, the present invention relates to techniques which can be applied effectively to a microcomputer incorporated in an IC card.

The so-called "IC card" has drawn an increasing attention in recent years as an improved replacement for magnetic cards such as those used with automated teller machines, credit cards, electronic locks, or the like. Such cards present encoded, machine-readable data, often tapered to a particular card carrier. In the magnetic cards, the information is generally encoded as a series of magnetic signals embedded on a ferric-type coating strip on the card.

The magnetic cards suffer from limited data storage capacity, as well as relative ease of access to the encoded data for unauthorized viewing or modification.

A first improvement to the magnetic card was presented by "memory cards." As disclosed in Japanese Patent Publication No. 19665/1981, typical memory cards incorporate therein a EPROM (ultraviolet "UV" erasable type programmable ROM) which stores data such as ID (identification) codes.

The EPROM memory cards suffer from an inability to allow for alterations to existing data. Erasure may

involve exposure of the entire chip to ultraviolet light of a predetermined strength, for a not insubstantial period of time. Such properties substantially impair the constant revisions and updates which are often desirable for stored data.

The IC card provides a means for substantially increasing the amount of data which may be stored, as well as allowing for selective modification thereof.

In addition, it is often desirable to include encryption or encoding schemes which will substantially impair unauthorized access to data stored on the IC card. Such serves to improve confidentiality of data to prevent unauthorized access to certain locations or to maintain integrity of information to be relied upon later. If a ROM device were to be used to accomplish encryption, an entire chip would have to be replaced periodically as the particular encryption schemes become known.

It is therefore desirable to provide a means for ease of semi-permanent storage of data, as well as a program allowing access thereto and manipulation thereof. It is also desirable to have a method for storage of and access to the data.

The present invention provides a microcomputer which can immediately satisfy diversified requirements for data storage and manipulation which includes the ability to semi-permanently preserve data as necessary. A preferred embodiment affords the ability to provide all functions on a single chip.

It is therefore an object of the present invention to provide technique which can improve the efficiency of hardware resources while keeping the advantages of the microcomputer described in that it can immediately satisfy diversified user's requirements for specification and application, and can further preserve semi-permanently data in EEP-ROM whenever necessary.

SUMMARY OF THE INVENTION

In accordance with the present invention there is provided a means for selective, semi-permanent storage of data or programs to a non-volatile memory. A central processing unit controls reads and writes of a program or data to the non-volatile memory in accordance with a data transfer program.

In accordance with another aspect of the present invention, a microcomputer which includes a non-volatile memory into which a user program and data may be written electrically, and a memory for storing a write control program for controlling the write operation to the non-volatile memory which is comprised of electrically programmable ROM ("EEP-ROM"). The EEP-ROM and the memory are disposed at mutually different positions on the address space of a CPU.

In accordance with a more limited aspect of the present invention, a program means for controlling the central processing unit to effect a write operation into the EEP-ROM is provided. In one embodiment, this program means is embedded in a mask ROM.

In accordance with another aspect of the present invention, the CPU is caused to jump to the memory containing the write control program only when data is to be written into the electrically writable ROM. The CPU can therefore execute a predetermined write control process during the write operation to the electrically writable ROM.

In accordance with another aspect of the present invention, the user program region and the data region are disposed in one electrically writable ROM and the proportion of the size of each region is arbitrarily selected. The scale of the hardware construction is

thereby reduced, and the utilization efficiency of the hardware resources are improved while keeping the advantages that various users' requirements for specifications and applications can be satisfied immediately. Additionally, data may be preserved semi-permanently in ROM as necessary.

BRIEF DESCRIPTION OF THE INVENTION

Fig. 1 is a block diagram showing the principal portions of a microcomputer with a built-in EEP-ROM;

Fig. 2 is a block diagram showing an example of the overall construction of the microcomputer shown in Fig. 1;

Fig. 3 is a block diagram showing the flow of data in the microcomputer shown in Fig. 2;

Fig. 4 is an address map showing three possible conditions of the address spaced of CPU in the microcomputer shown in Fig. 2;

Fig. 5 is a flowchart showing an example of the operation of the microcomputer shown in Fig. 2;

Fig. 6 is a block diagram showing the construction of the micrcomputer with a built-in EEP-ROM in an alternate embodiment of the present invention;

Fig. 7 is a block diagram showing the flow of data in the microcomputer shown in Fig. 6; and

Fig. 8 is an address map showing the conditions of the address space of CPU in the microcomputer shown in Fig. 6.

DESCRIPTION OF THE PREFERRED AND ALTERNATE EMBODIMENTS

Hereinafter, various embodiments of the present invention will be described with reference to the

accompanying drawings. Like reference numerals will be used throughout the drawings to identify the same or like constituents.

Fig. 1 shows the principal portions of the micrcomputer 10 in accordance with one embodiment of the present invention. The microcomputer is designed to provide data transfer to and from a contiguous memory as will be described below. Data transfer operations include reads or writes to or from the memory, movement of data from one memory location to another, or revision of stored data in accordance with other data.

Data transfers are made in conjunction with an external data device, which may be a data source, which the microcomputer operates. Suitable means are provided, such as a parallel interface, a serial interface, or an edge card connector, to place the microcomputer in data communication therewith.

The microcomputer 10, whose principal portions are shown in Fig. 1, is of a single chip type. Included is a CPU 1, and EEP-ROM 4 into which both a user program Ix2 and data to be preserved are written in arbitrary proportion. The micrcomputer 10 also includes a so-called mask ROM 3 which has fixed therein a program for effecting a write control operation of a data transfer which provides for writing and overwriting of data into EEP-ROM 4. This is part of the standard program Ix1. Generally, the time necessary for the write operation to EEP-ROM is about 1,000 times a mean instruction execution time of the CPU.

Mask ROMs can generally be fabricated in a smaller area than EEP-ROMs having the same capacity. Accordingly, overall size of the semiconductor chip can be reduced by utilizing the mask ROM 3 instead of storing all the programs in EEP-ROM 4. Additionally,

mask ROM 3 may store only the write control program or may store the aforementioned standard program routine.

The write control program includes a program for starting operation of the write control circuit 7 or a program for detecting completion of the write operation. EEP-ROM 4 and mask ROM 3 are disposed at mutually different address positions on the address space of CPU 1.

The switch shown in Fig. 1 is illustrative only, and is used to identify that a program controlling execution of the CPU 1 is tranferred to mask ROM 3 by a call instruction at the time of a write operation, and is returned to a program in EEP-ROM 4 by return instruction after completion of the write operation.

A call instruction to a specific routine in the mask ROM 3 can be written into EEP-ROM 4 in place of the write control program to EEP-ROM 4. Correspondingly, a return instruction to EEP-ROM 4 can be written at the end of the write control program into the mask ROM 3 together with the write control program for EEP-ROM 4.

Fig. 2 shows one embodiment of the overall construction of the microcomputer 10 shown in Fig. 1. As shown in the drawing, the microcomputer 10 incorporates therein, in addition to the elements of Fig. 1, a RAM 2 providing the work region of CPU 1, an I/O unit (input/output unit) 5 for the exchange of the data Dx to and from the outside, a peripheral circuit 6, and an EEP-ROM write control unit 7. Since the microcomputer includes these constituent elements, it is suitable as a single chip type microcomputer to be incorporated in the IC card. These units (1, 7) of the microcomputer 10 are connected to one another through an address bus AD and a data bus LD.

As noted above, the RAM 2 provides a work region or scratch pad of easily readable and writable RAM for use of the central processing unit. If the quantity of the data to be written is great, the data prepared in a predetermined region in RAM 2 overflow may be transferred sequentially to EEP-ROM 4. Such is accomplished under the control of either the standard program or the user program.

Control signals for the memories and suitable peripheral circuits are well within the abilities of one of ordinary skill in the art, and are omitted from the drawing for ease of illustration.

Fig. 3 shows the flow of data Dx in the microcomputer of Fig. 2. As shown in the drawing, the exchange of data Dx to and from the outside is effected through the CPU 1. Therefore, the built-in software cannot be accessed unless a "key" of suitable software is used.

Fig. 4 shows three possible address apportionments of memory, illustrated by memory maps. As shown in the drawing, both the user program region M1 and the data region M2 are allotted in a suitable proportion to the memory region M of EEP-ROM 4.

Fig. 5 shows the flowchart of an example of the processing operation as a write control for EEP-ROM 4 is made called for by CPU 1.

In Fig. 2 and Fig. 5 the CPU 1 reads, instruction by instruction, the program Ix2 written into the user program region M1 and executes a predetermined processing operation (step S6).

If it becomes necessary to preserve data Dx into EEP-ROM 4 during this process (step S1), the CPU 1 jumps to the leading address of the write control program in the standard program region Ix1, preferably

stored in mask ROM 3, by call a instruction (step S2). The write control processing of EEP-ROM 4 is executed in accordance with the write control program (step S3). In this manner, a write to EEP-ROM 4 is conducted through the EEP-ROM write control unit 7. During this write operation, the EEP-ROM 4 is electrically isolated from the CPU 1 by a suitable electric switch or gate means, such as a tri-state buffer.

The CPU 1 judges completion of the write operation on the basis of a flag generated from the write control unit 7, or an interrupt request (step 4). Then, CPU 1 returns from mask ROM 3 to the program region M1 of EEP-ROM 4 and recommences the read operation of the user program from next address to the address at the time of jump (step S5). CPU 1 keeps executing the user program until the processing is complete or until a next data write request occurs (step S6).

As described above, the user program region M1 and the data region M2 are preferably disposed in one EEP-ROM 4. At the same time, since the sizes of both regions M1 and M2 can be varied in proportion. The memory region M can be interchanged and used efficiently between the user program region M1 and the data region M2 by, for example, increasing the size of the program region M1 and reducing the size of the data region M2 or vice versa, as can be seen from the three examples shown in Fig. 4. Such an apportionment provides for functionality of the device even if the size of the memory region M of EEP-ROM as a whole is not substantial.

Accordingly, the present invention allows for the construction scale of the hardware to be reduced, and efficient utilization of hardware resources, while advantageously providing for immediate satisfaction of

user's diversified specifications. Data can be also preserved semi-permanently in EEP-ROM 4 as may be necessary.

It should be noted that the return to the user program upon completion of the write operation to EEP-ROM need not use the flag generated from the write control unit 7, or the interrupt request, as in the embodiment described above. For example, it is possible to employ a circuit construction wherein a suitable work register in CPU 1 is operated simultaneously with the start of a write operation to EEP-ROM, and is used as a counter or timer which is updated in a predetermined period during its operation. A return operation is then executed when the content of such a work register reaches a predetermined value. In other words, a construction is envisioned wherein CPU 1 counts a predicted and predetermined write time and checks, by means of a software, the point of completion of the write operation to EEP-ROM. In this case, setting of the write time and the control of the subsequent return operation can be made by means of hardware using a dedicated circuit, such as a timer circuit.

The user program in the embodiment described above further includes a construction wherein the CPU 1 is stopped by an external control and the write operation is directly made to the user program region M1 of EEP-ROM 3 from an exterior data source with which the CPU is in data communcation.

This write operation of the user program may be effected by a construction wherein the CPU 1 receives a program from outside through the I/O unit 5 in accordance with the program of mask ROM 3, and then makes the write operation to the user program region M1 of EEP-ROM 4. Since such a use does not allow direct

access to the built-in EEP-ROM 4 from outside, the function of keeping secrecy is improved and the suitability of the microcomputer for the single chip type microcomputer to be incorporated in the IC card is further improved.

Whether or not the write operation to the user program 4 has already been made is judged by a flag which is disposed inside EEP-ROM 4. The start address after reset of CPU 1 can also be changed in accordance with the status of this flag.

It will be appreciated that while EEP-ROMs are desirable as non-volatile memory, the above-described organization may be implemented in UV-EPROM memory.

In the embodiment described above, the write operation is made by the write control circuit 7 for a predetermined period, though other analagous methods may be employed.

An alternate embodiment of a suitable microcomputer shown in Fig. 6. This embodiment is of a single chip type with a built-in EEP-ROM, and includes a CPU (central processing unit) 1, RAM (random access memory) 2, mask ROM (fixed memory ROM) 3, EEP-ROMs 41, 42, I/O (input/output unit) 5, peripheral circuit 6 and EEP-ROM write control unit 7 inside the same semiconductor chip. Each unit (1, 7) is connected to the other by address bus LA and data bus LD.

This single chip type microcomputer 10 may be used in conjunction with an IC card. The exchange of data Dx to and from outside is all effected through CPU 1 as shown in Fig. 7. Also shown is the flow of data Dx in the microcomputer 10 of Fig. 6 This microcomputer can similarly be implemented in such a fashion that unless a "key" of a suitable software in the EEP-ROM or the CPU is used, the built-in software cannot be accessed.

In Figs. 6 and 7, EEP-ROMs 41 and 42 are generally equivalent, and are disposed independently of each other. One (41) of them is used as a so-called "user program region" (M1) as shown in Fig. 8, into which a program, prepared freely by the user, can be written in advance. A write operation of this program is made by stopping the CPU from an external control signal and writing the data directly into EEP-ROM 41. A suitable programming method for such a PROM is found in "Hitachi Microcomputer Data Book, 8-bit Single Chip", pp. 823 - 865, published in August, 1984 by Hitachi, Ltd., which is incorporated herein by reference. This alternate embodiment advantageously eliminates the necessity for rewriting the mask ROM in the production process, and can cope instantly with the diversified applications by the users.

Furthermore, suitable means may be provided to inhibit re-write or read to and from this EEP-ROM 41 after programming is finished. This allows the built-in software to be protected effectively. The other EEP-ROM 42 is used as a data region (M2). Here, those data Dx which must be preserved among the input/output data managed by CPU 1 are written instantaneously whenever necessary. A write operation to this EEP-ROM 42 is effected through a write control circuit 7 which is controlled by CPU 1. During this write period, EEP-ROM 42 is electrically cut off from CPU 1 and both write and read operations to and from EEP-ROM 42 are not possible.

The CPU 1 reads, instruction by instruction, a user program Ix2 stored in the program storage EEP-ROM 41, and executes a predetermined processing operation. When it becomes necessary during this processing to write preservation data Dx into the data storage EEP-ROM 42, a write operation to this EEP-ROM 42 is made through

the EEP-ROM write control unit 7. During execution of the Ix2 program, reference is made, whenever necessary, to a second program routine (or a program module) prepared in advance as a standard program Ix1. This second program is stored in the mask ROM 3. The Ix1 program routine may comprise a software timer, a division program, or other various programs prepared in accordance with various intended applications. Overall processing is, however, conducted in accordance with the user program written into EEP-ROM 41.

The EEP-ROM write control unit 7 shown in Fig. 7 makes a write operation to the EEP-ROM 42 under the controlled of the program written into one of the EEP-ROMs. The remaining EEP-ROM 42 is, similarly to the preferred embodiment, electrically cut off from CPU 1 while the write operation is being carried out by its counterpart.

The microcomputer 10 of the alternate embodiment described above requires two mutually independent EEP-ROMs 41 and 42 in order to write the user program Ix2 and to store the data Dx to be preserved. If only one EEP-ROM is used, read access to the EEP-ROM cannot be made while the write operation is made to it, as the next instruction to be executed by CPU 1 cannot then be read out. The program and the data are therefore stored in the mutually independent EEP-ROMs 41 and 42. While the instruction is being read out from one (41) of the EEP-ROMs, the write control of the other (42) is made on the basis of the instruction read out from the former.

Since in this embodiment, the two mutually independent EEP-ROMs 41, 42 must be used in order to satisfy diversified user's requirements for specifications, both must be large enough to handle all

applications. This capacity is necessary to satisfy such requirements as large program size, even though data storage requirements may be small, or alternatively, large data storage requirements, though the program size may be small. Even if both EEP-ROMs 41, 42 have a sufficient memory capacity, the memory capacity is not always used fully and hence waste is likely to occur.

Each of these EEP-ROMs 41, 42 includes a sense amplifier, circuits for data input/output such as a driver circuit, and a peripheral circuit consisting of an address selection circuit with its corresponding memory array. Therefore, if a plurality of EEP-ROMs are formed independently of one another, peripheral circuits such as the sense amplifier and the driver must be disposed inside the respective EEP-ROM. Hence, a greater number of circuit elements become necessary and increase the overall size of EEP-ROM.

A variation to the alternate embodiment includes storage, in EEP-ROM 41 the control program for EEP-ROM 42 and the data to be referred to by the program of EEP-ROM 42, and storage in EEP-ROM 42 the control program for EEP-ROM 41 and the data to be referred to by the program of EEP-ROM 41. Such allows the program storage area and the data storage area in each of EEP-ROMs 41, 42 to become variable. In this case, the afore-mentioned problem of the memory area or size is somewhat mitigated. In this case, however, each EEP-ROM 41, 42 must have the independent peripheral circuits such as the sense amplifier and the decoder circuit, and overall circuit size is increased.

The write time in EP-ROMs in general is longer than in EEP-ROMs. Accordingly, if the write time is constant as in the embodiment described above, the

response time will increase when the microcomputer is incorporated in the IC card. In this case, an unnecessarily long write time is necessary because the write time is set in consideration of a worst case, due to process variances of EP-ROM devices.

It is contemplated that a long write time may be improved by improving the above write control program.

Among the effects brought forth by the preferred embodiment of the present invention, the following will describe typical examples.

In a microcomputer with a built-in EEP-ROM, the user program region and the data region can be dispoed in one EEP-ROM and their sizes can be selected in proportion. Accordingly, the scale of the hardware construction can be reduced and the utilization efficiency of the hardware resources can be improved while keeping the advantages that various users' requirements for specifications and applications can be immediately satisfied, and the data Dx can be preserved semi-permanently in EEP-ROM whenever necessary.

When the present invention is applied to a single chip type microcomputer to be incorporated in the IC card, the strength of the IC card can be improved due to the reduction of the size of the semiconductor chip.

Although the present invention has thus been described with reference to the preferred embodiment thereof, the invention is not particularly limited thereto but can be changed or modified in various forms without departing from the scope and spirit thereof. For example, when the write control program is stored in advance in mask ROM 3 or EEP-ROM 4 and when the write operation to EEP-ROM 4 is made, the write control program may be tranferred to RAM 2 in order to let CPU 1 execute it.

Although the description given above illustrates the example wherein the present invention is applied to the single chip type microcomputer for the IC card, the present invention is not particularly limited thereto but can be applied, too, to a board type microcomputer.

In other words, the present invention can be applied to microcomputers of the type wherein the program and the data are stored at least in EEP-ROM.

What is claimed is:

1. A microcomputer comprising:

a central processing unit having memory address space;

a non-volatile storage means for storing at least one of a program and data under direction of said central processing unit;

memory means for storing a data transfer program for controlling the central processing unit to effect a data transfer operation to said non-volatile storage means, said non-volatile storage means and said memory means being disposed at different address positions on the memory address space of said central processing unit;

means for placing said central processing unit in data communication with an associated exterior data device; and

means for effecting a data transfer in accordance with signals from said associated exterior data device.

2. A microcomputer according to claim 1, wherein at least a portion of said memory for storing said data transfer program is mask ROM.

3. A microcomputer according to claim 1, wherein at least a portion of said memory for storing said data transfer program is RAM.

4. A microcomputer according to claim 1, wherein said non-volatile storage means includes gate means for disabling transfer of at least one of an address and data from said central processing unit to said non-volatile storage means during write period of said data transfer.

5. A microcomputer according to claim 2, wherein said non-volatile storage means is a single EEP-ROM.

6. A microcomputer according to claim 2, wherein said non-volatile storage means is a single EP-ROM.

7. A microcomputer according to claim 5, wherein said non-volatile storage means includes gate means for disabling transfer of at least one of an address and data from said central processing unit to said non-volatile storage means during a write period of said data transfer.

8. A microcomputer according to claim 1, wherein all constituent elements are implemented in a large-scale-integration semiconductor device.

9. A microcomputer comprising:

a central processing unit having memory address space;

an electrically programmable ROM into which both program and data can be written under direction of said central processing unit;

a memory for storing a write control program for controlling a write operation to said electrically programmable ROM;

a write control means for controlling the write operation to said electrically programmable ROM;

said electrically programmable ROM and said memory being disposed at mutually different address positions on the address space of said central processing unit.

10. A microcomputer according to claim 9, wherein said write control means includes a latch means for retaining control signals to said electrically programmable ROM during a write period.

11. A microcomputer according to claim 9, wherein all constituent elements are implemented in a large-scale-integrated semiconductor device.

12. In a microcomputer comprising a central processing unit, an electrically programmable ROM in which both program and data can be written and a memory for storing a write control program, a method of writing data to said electrically programmable ROM, said method comprising the steps of:

(1) causing said central processing unit to jump from a program in said electrically programmable EP-ROM to a leading address of a write control program in said memory;

(2) executing a write control process in said electrically programmable ROM under the write control program;

(3) judging completion of the write operation in said central processsing unit;

(4) returing said central processing unit from said memory to a program in said electrically programmable ROM.

13. The method of writing data according to claim 12, further comprising a step of controlling the judging by a flag generated from at least one of a write control unit and an interrupt request.

14. A semiconductor integrated circuit device comprising:

a non-volatile storage means into which both program and data can be written;

a memory for storing a write control program for controlling a write operation to said non-volatile storage means;

control means having address space for controlling said non-volatile storage means and said memory; and

said non-volatile storage means and said memory being disposed at mutually different address positions on the address space of said control means.

15. A semiconductor integrated circuit device according to claim 14, wherein said memory for storing said write control program is ROM.

16. A semiconductor integrated circuit device according to claim 14, wherein said memory for storing said write control program is mask RAM.

17. A semiconductor integrated circuit device according to claim 14, wherein said control means is a central processing unit.

18. A semiconductor integrated circuit device according to claim 14, wherein said non-volatile storage means includes gate means for disabling transfer of at least one of an address and data input from said control means to said non-volatile storage means during the write operation.

19. A semiconductor integrated circuit device according to claim 14, wherein said non-volatile storage means is a single EEP-ROM.

20. A semiconductor integrated circuit device according to claim 14, wherein said non-volatile storage means is a single EP-ROM.

FIG. 3

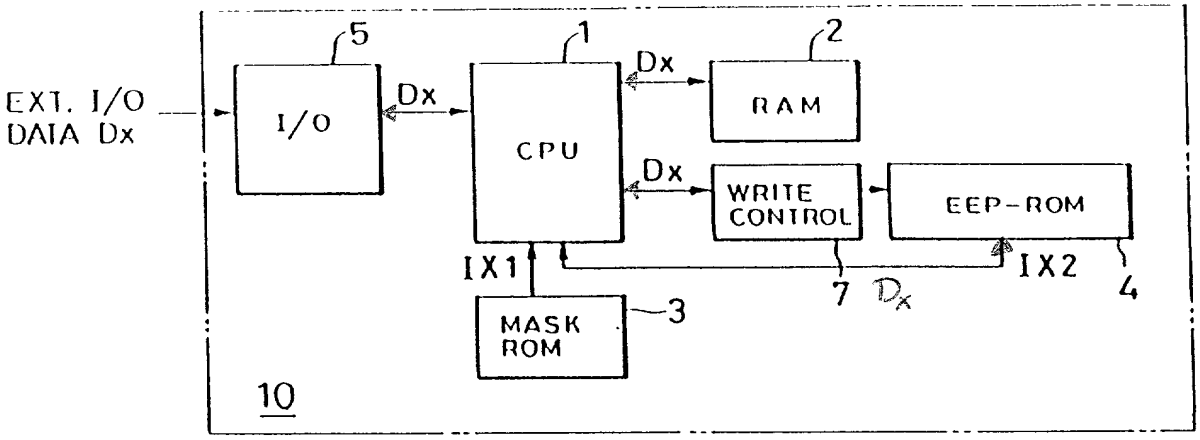

EXT. I/O
DATA Dx
5
I/O
Dx
1
CPU
Dx
2
RAM
Dx
WRITE
CONTROL
EEP-ROM
IX1
7 Dx
IX2
4
MASK
ROM
3
10

FIG. 4

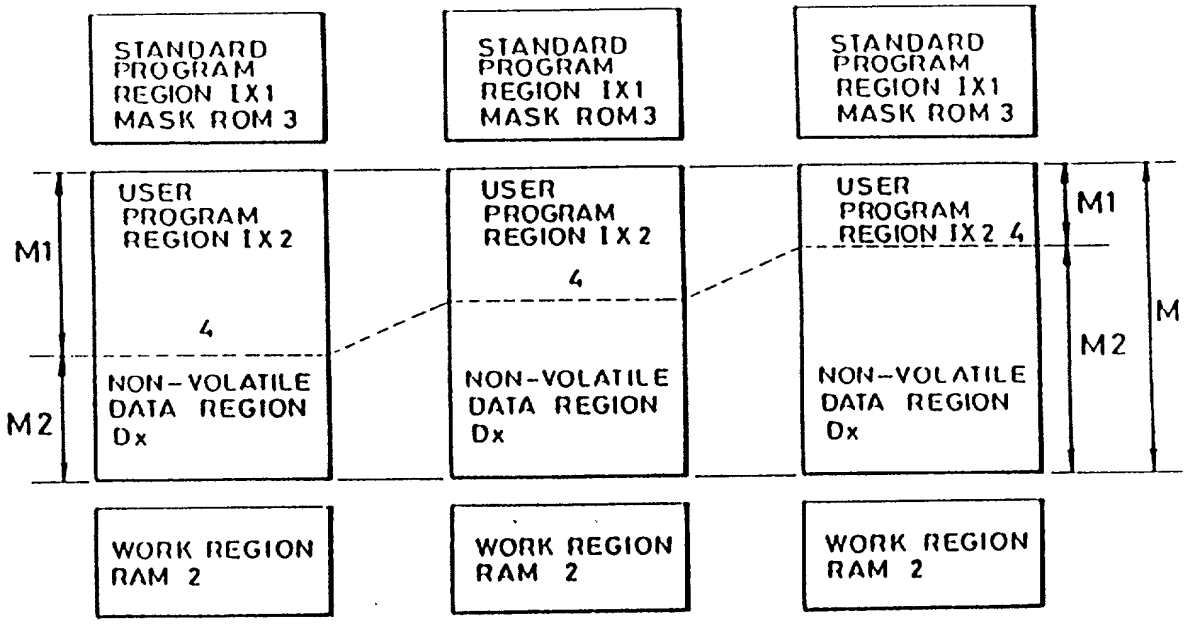

STANDARD
PROGRAM
REGION IX1
MASK ROM 3
STANDARD
PROGRAM
REGION IX1
MASK ROM3
STANDARD
PROGRAM
REGION IX1
MASK ROM 3
M1
M2
USER
PROGRAM
REGION IX2
4
NON-VOLATILE
DATA REGION
Dx
USER
PROGRAM
REGION IX2
4
NON-VOLATILE
DATA REGION
Dx
USER
PROGRAM
REGION IX2 4
M1
M2
M
NON-VOLATILE
DATA REGION
Dx
WORK REGION
RAM 2
WORK REGION
RAM 2
WORK REGION
RAM 2

FIG. 6

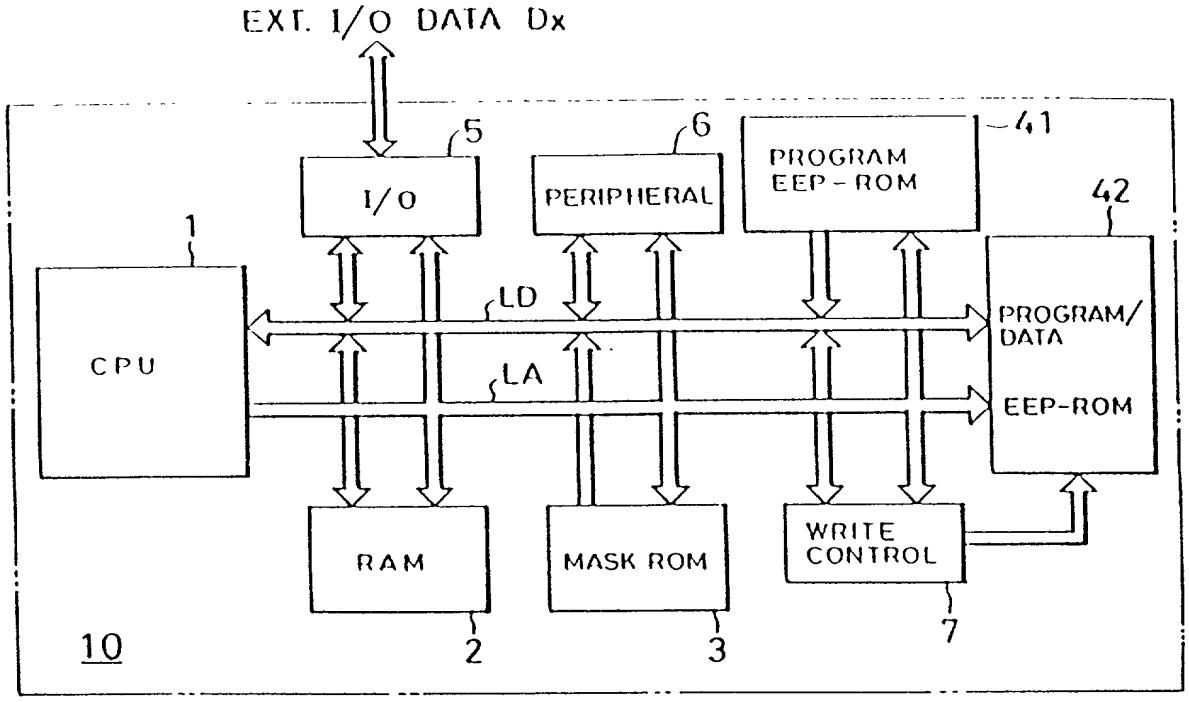

EXT. I/O DATA Dx
I/O
5
PERIPHERAL
6
PROGRAM EEP-ROM
41
42
1
CPU
LD
LA
PROGRAM/ DATA
EEP-ROM
RAM
MASK ROM
WRITE CONTROL
2
3
7
10

FIG. 7

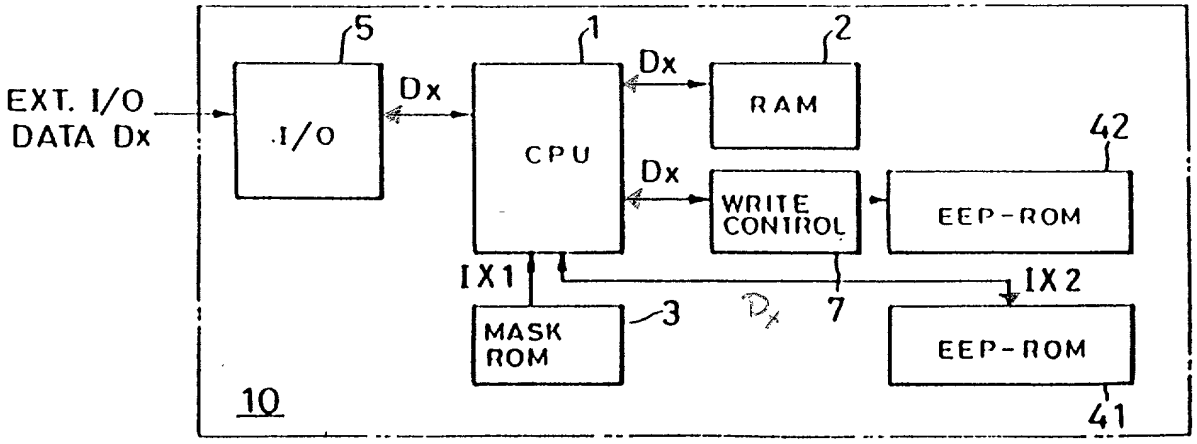

EXT. I/O DATA Dx
5
I/O
Dx
1
CPU
Dx
2
RAM
Dx
WRITE CONTROL
42
EEP-ROM
IX1
IX2
MASK ROM
3
Dx
7
EEP-ROM
41
10

FIG. 3

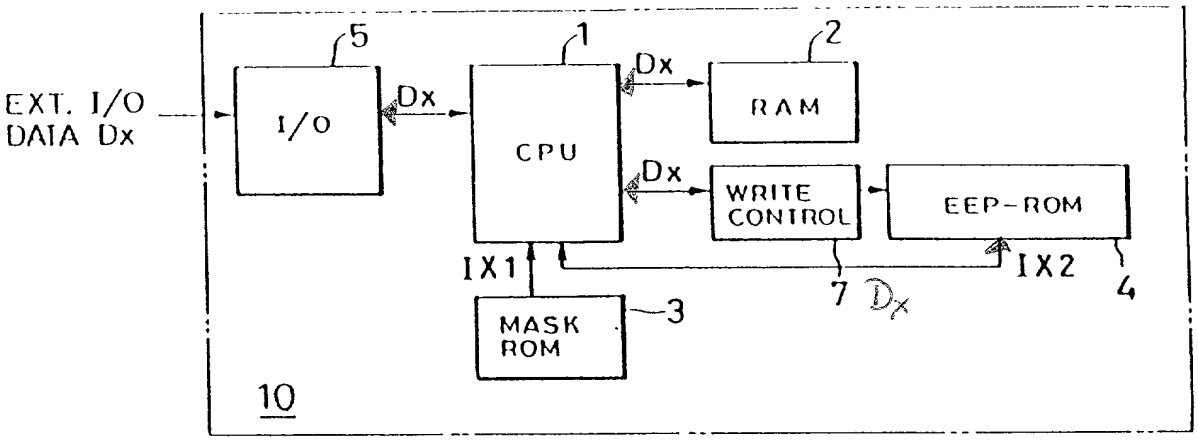

EXT. I/O
DATA Dx
5
I/O
Dx
1
CPU
Dx
2
RAM
Dx
WRITE
CONTROL
EEP-ROM
IX1
IX2
7 Dx
4
MASK
ROM
3
10

FIG. 4

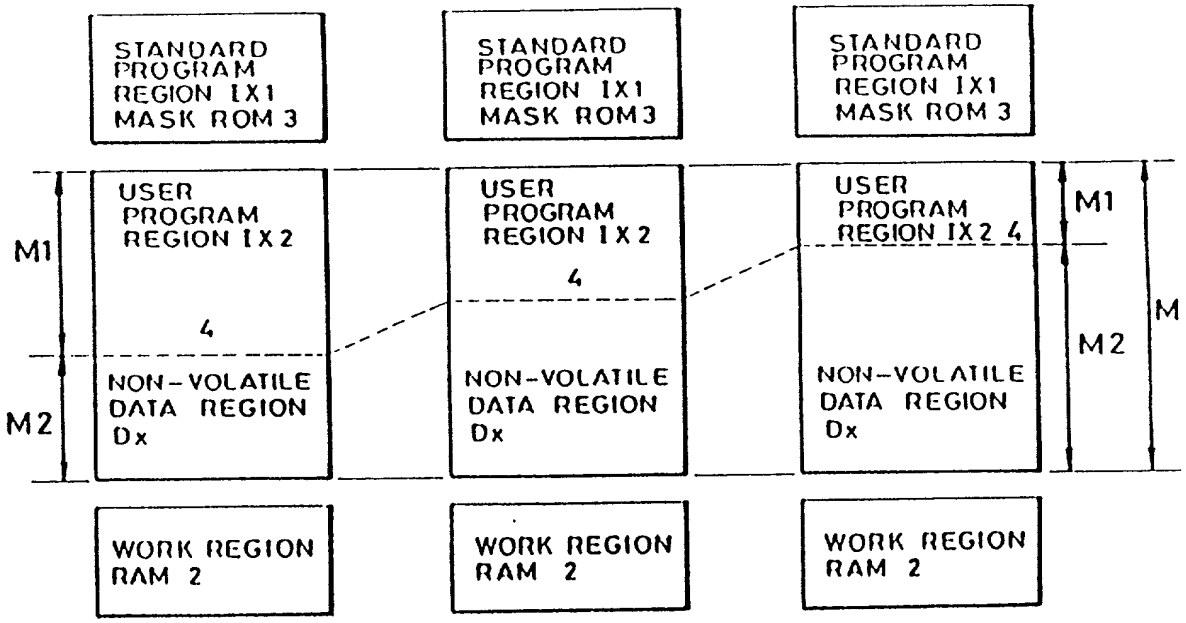

STANDARD
PROGRAM
REGION IX1
MASK ROM 3
STANDARD
PROGRAM
REGION IX1
MASK ROM3
STANDARD
PROGRAM
REGION IX1
MASK ROM 3
M1
M2
USER
PROGRAM
REGION IX2
4
NON-VOLATILE
DATA REGION
Dx
USER
PROGRAM
REGION IX2
4
NON-VOLATILE
DATA REGION
Dx
USER
PROGRAM
REGION IX2 4
NON-VOLATILE
DATA REGION
Dx
M1
M2
M
WORK REGION
RAM 2
WORK REGION
RAM 2
WORK REGION
RAM 2

FIG. 6

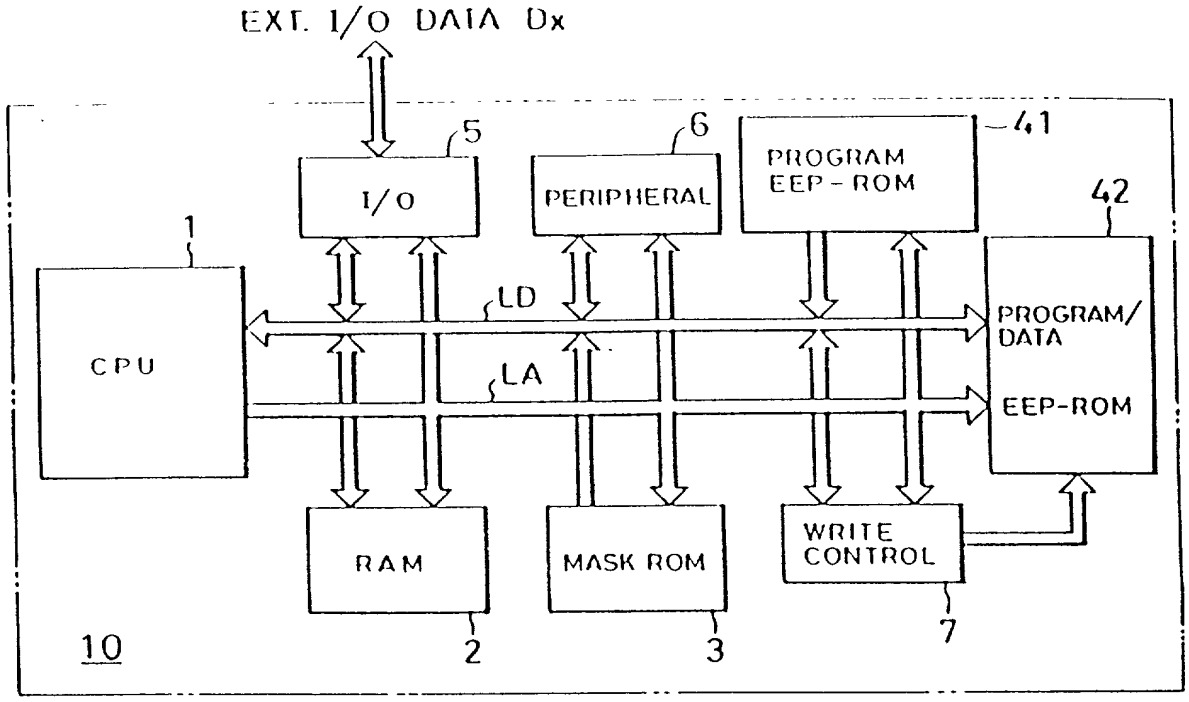

EXT. I/O DATA Dx
I/O
5
PERIPHERAL
6
PROGRAM EEP-ROM
41
42
1
CPU
LD
LA
PROGRAM/ DATA
EEP-ROM
RAM
MASK ROM
WRITE CONTROL
2
3
7
10

FIG. 7

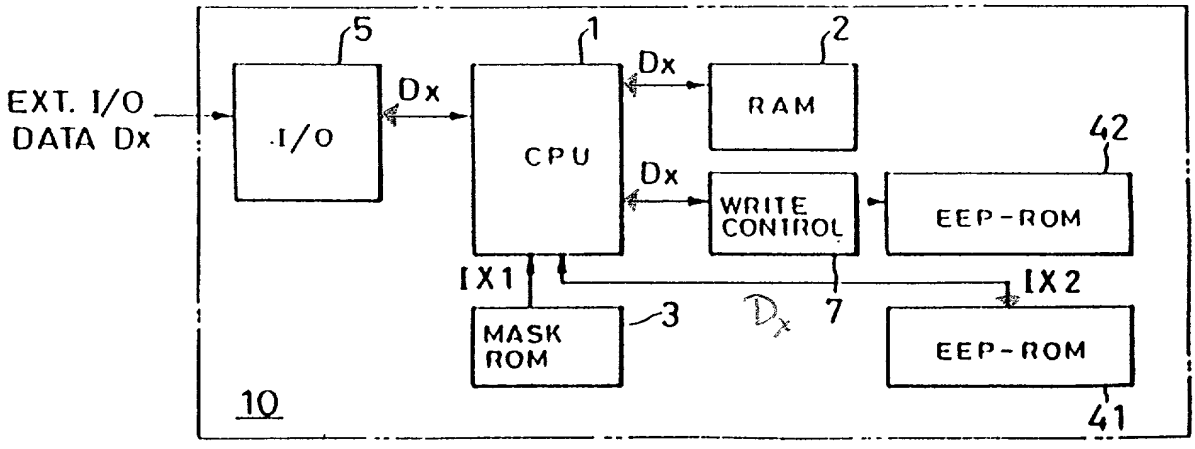

EXT. I/O DATA Dx
5
I/O
Dx
1
CPU
Dx
2
RAM
Dx
WRITE CONTROL
42
EEP-ROM
IX1
IX2
MASK ROM
3
Dx
7
EEP-ROM
41
10

FIG. 1

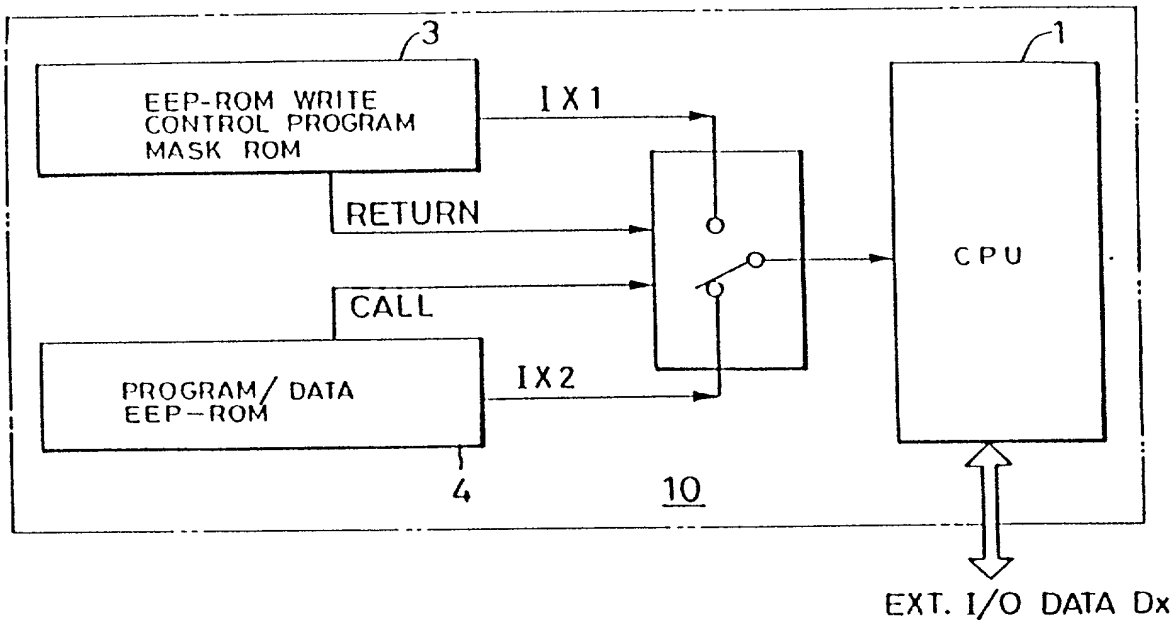

3
EEP-ROM WRITE CONTROL PROGRAM MASK ROM
IX1
RETURN
CALL
PROGRAM/ DATA EEP-ROM
IX2
4
10
1
CPU
EXT. I/O DATA Dx

FIG. 2

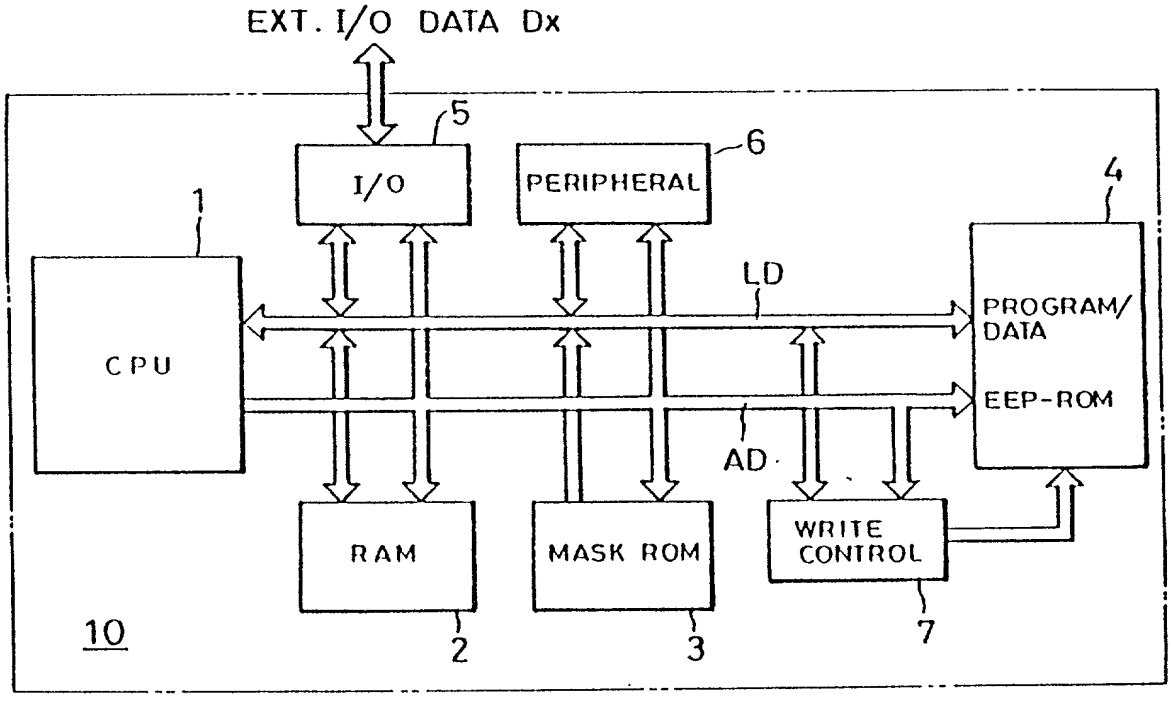

EXT. I/O DATA Dx
5
I/O
PERIPHERAL
6
4
1
CPU
LD
PROGRAM/ DATA
EEP-ROM
AD
RAM
MASK ROM
WRITE CONTROL
10
2
3
7

FIG. 3

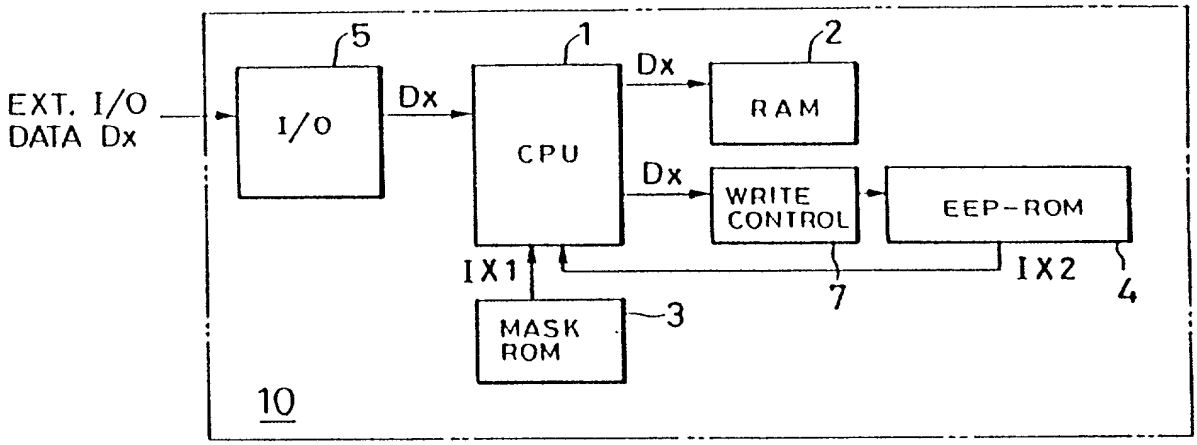

EXT. I/O
DATA Dx
5
I/O
Dx
1
CPU
Dx
2
RAM
Dx
WRITE
CONTROL
EEP-ROM
IX1
IX2
7
4
MASK
ROM
3
10

FIG. 4

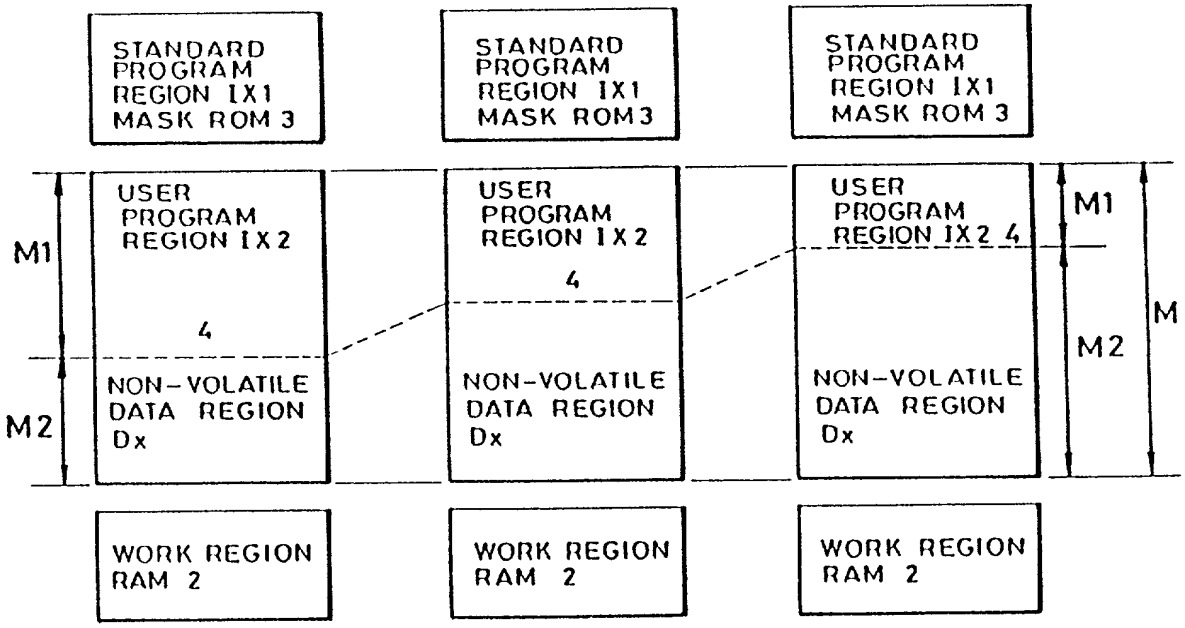

STANDARD
PROGRAM
REGION IX1
MASK ROM 3
STANDARD
PROGRAM
REGION IX1
MASK ROM3
STANDARD
PROGRAM
REGION IX1
MASK ROM 3
M1
M2
USER
PROGRAM
REGION IX2
4
NON-VOLATILE
DATA REGION
Dx
USER
PROGRAM
REGION IX2
4
NON-VOLATILE
DATA REGION
Dx
USER
PROGRAM
REGION IX2 4
NON-VOLATILE
DATA REGION
Dx
M1
M2
M
WORK REGION
RAM 2
WORK REGION
RAM 2
WORK REGION
RAM 2

FIG. 5

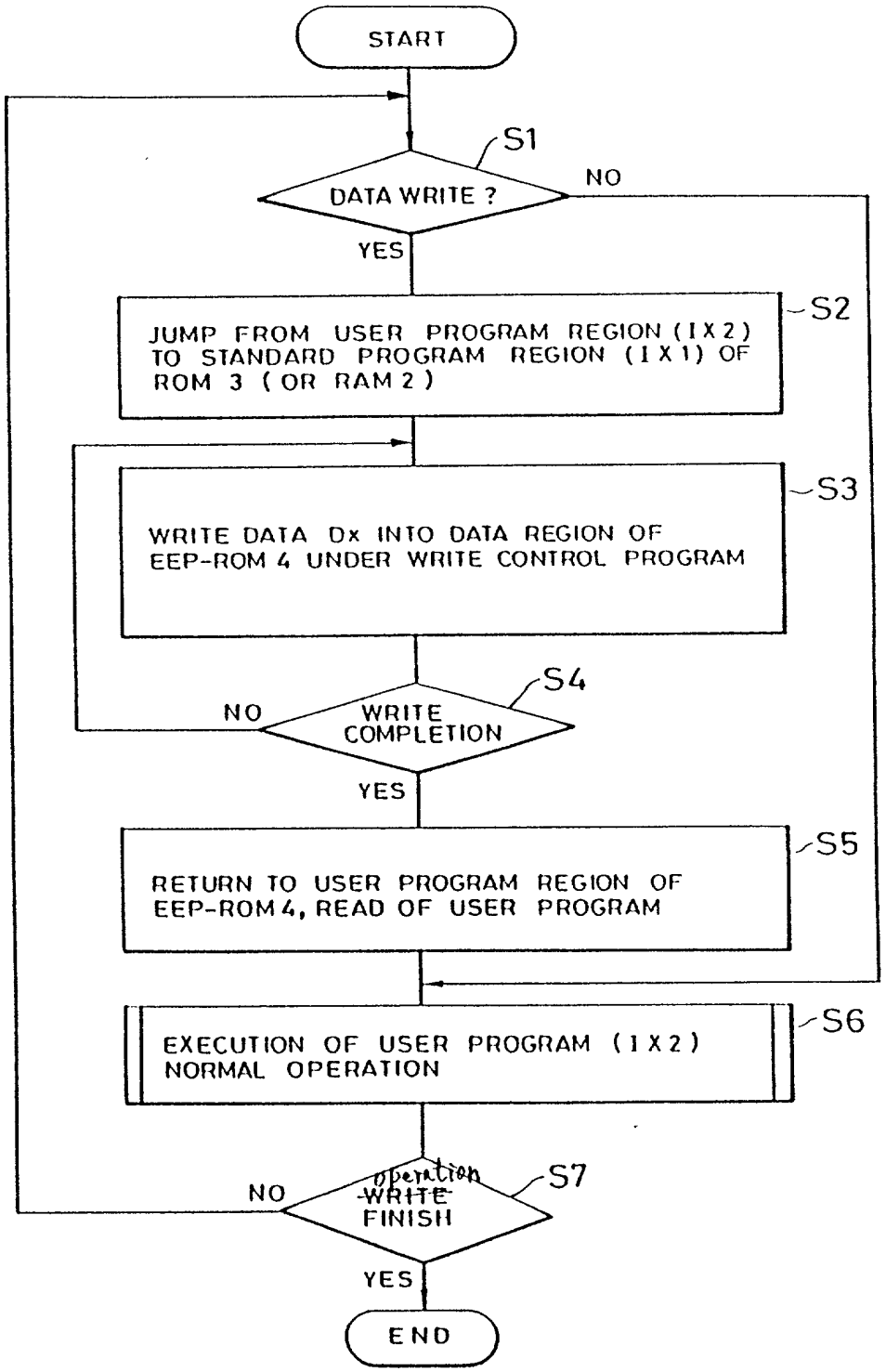

START
S1
DATA WRITE ?
NO
YES
JUMP FROM USER PROGRAM REGION (1X2) TO STANDARD PROGRAM REGION (1X1) OF ROM 3 (OR RAM 2)
S2
WRITE DATA Dx INTO DATA REGION OF EEP-ROM 4 UNDER WRITE CONTROL PROGRAM
S3
S4
NO
WRITE COMPLETION
YES
RETURN TO USER PROGRAM REGION OF EEP-ROM 4, READ OF USER PROGRAM
S5
EXECUTION OF USER PROGRAM (1X2) NORMAL OPERATION
S6
NO
operation
~~WRITE~~ FINISH
S7
YES
END

FIG. 6

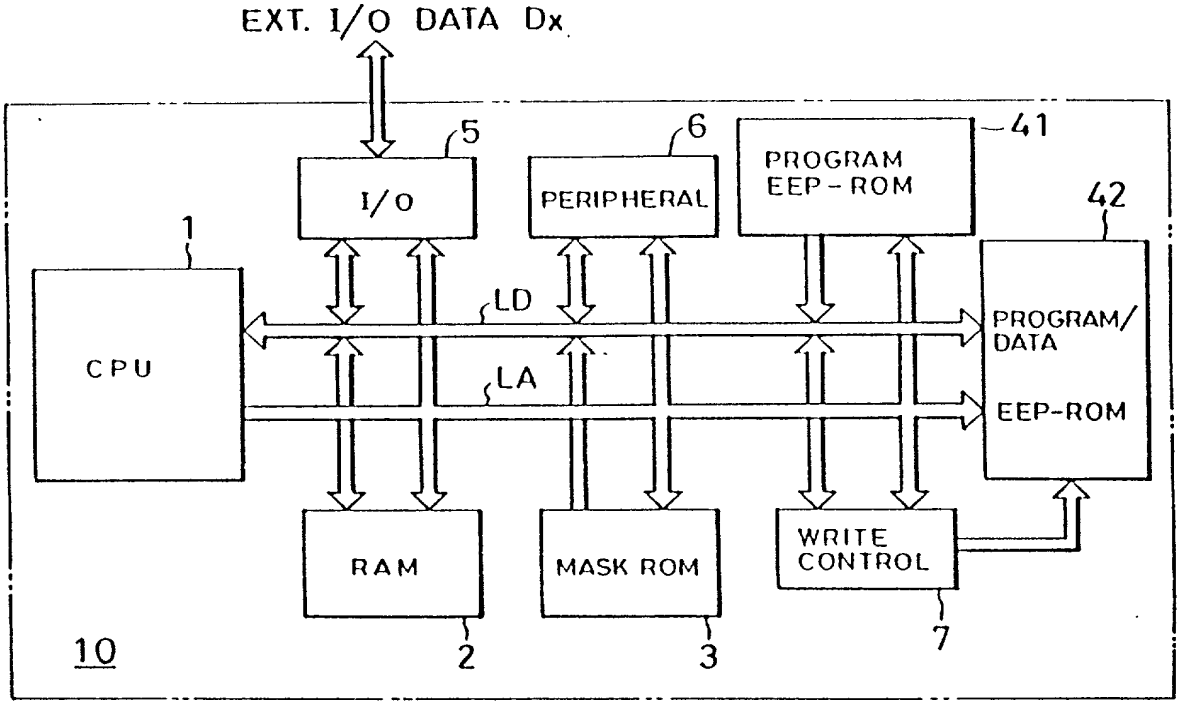

EXT. I/O DATA Dx
5
6
41
I/O
PERIPHERAL
PROGRAM EEP-ROM
42
1
CPU
LD
LA
PROGRAM/ DATA
EEP-ROM
RAM
MASK ROM
WRITE CONTROL
10
2
3
7

FIG. 7

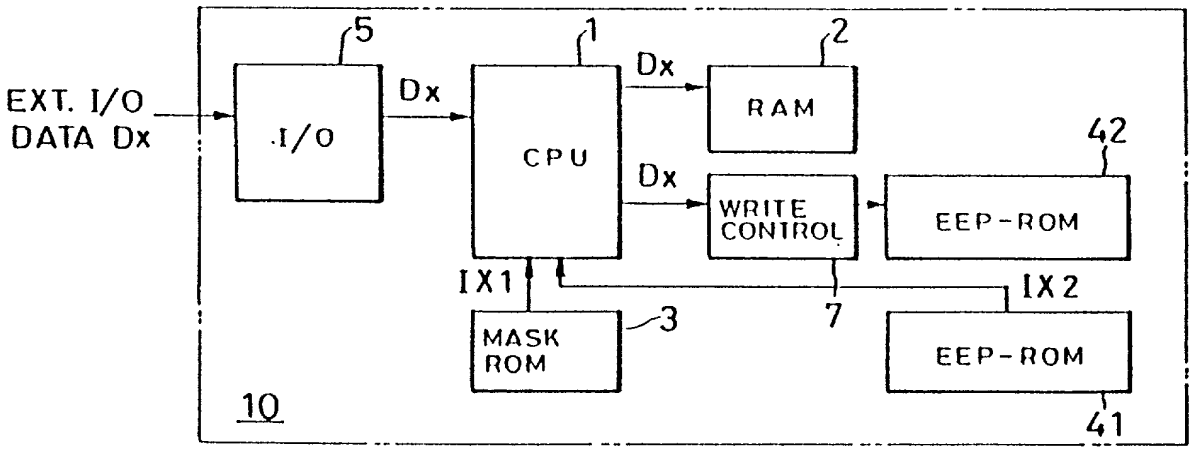

EXT. I/O DATA Dx
5
1
2
I/O
Dx
CPU
Dx
RAM
Dx
42
WRITE CONTROL
EEP-ROM
IX1
IX2
MASK ROM
3
7
EEP-ROM
10
41

FIG. 8

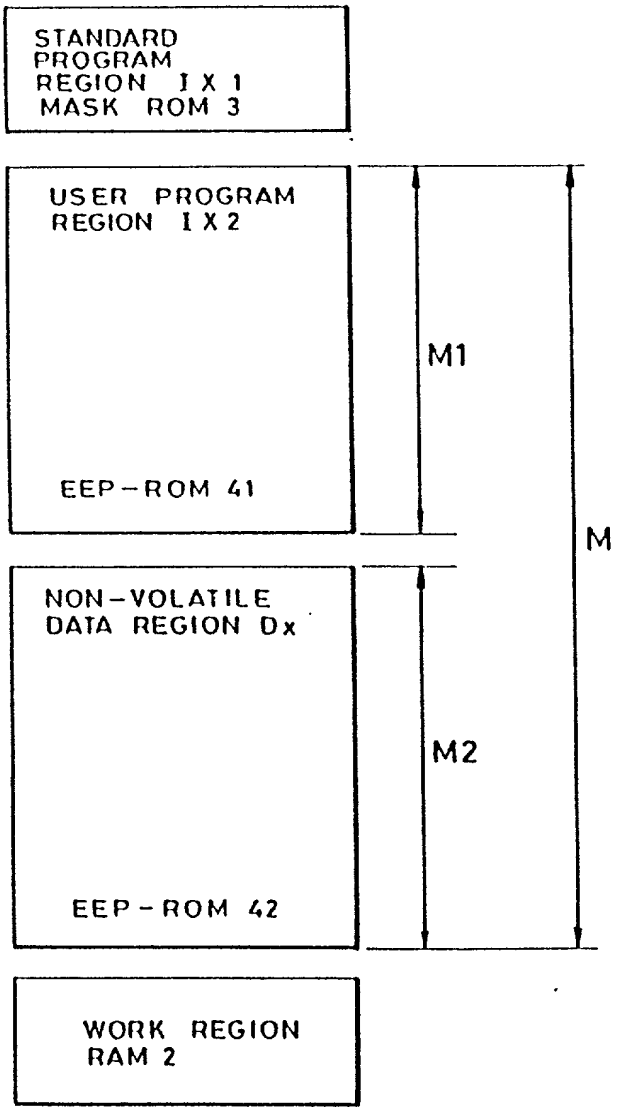
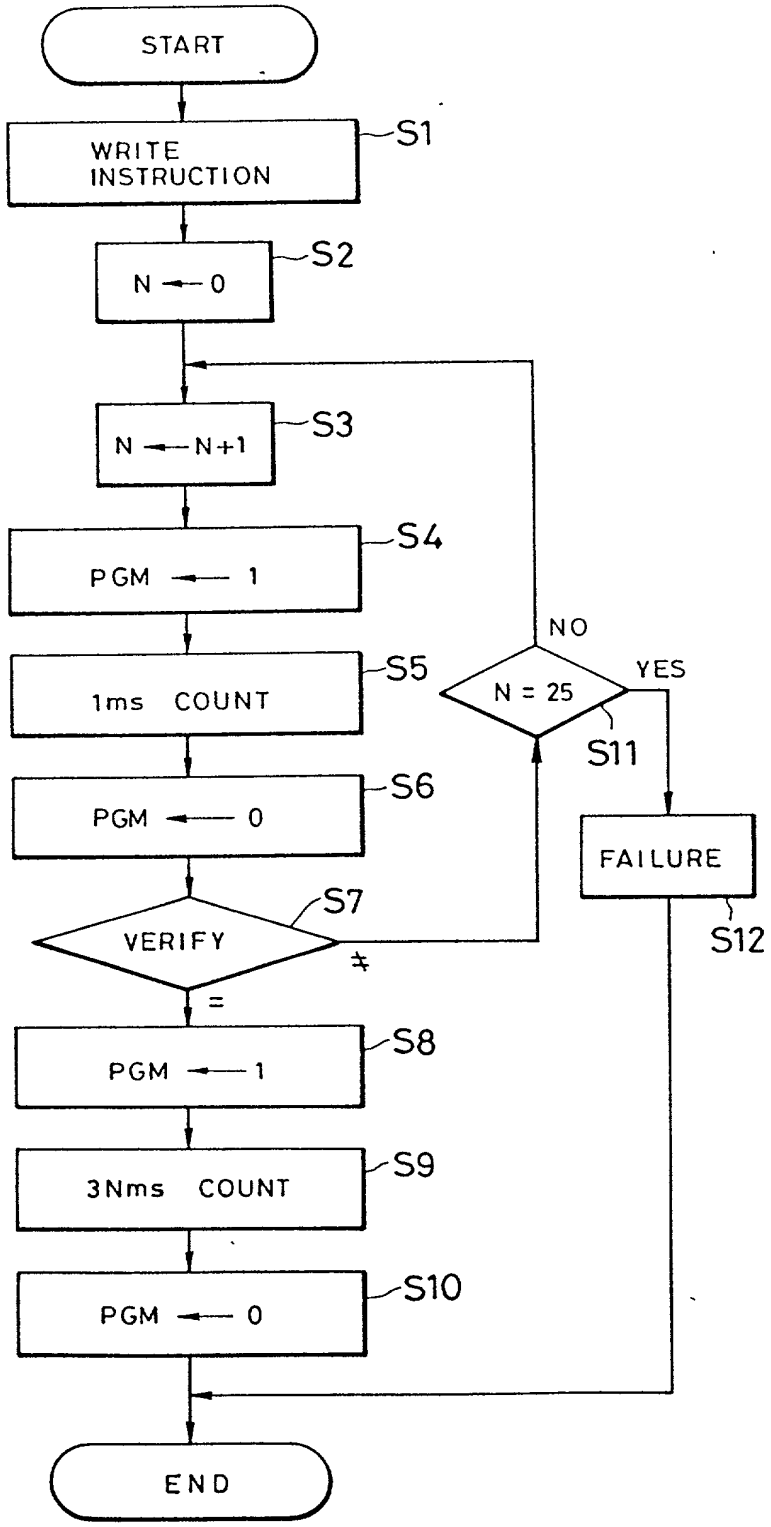

STANDARD PROGRAM REGION IX1 MASK ROM 3
USER PROGRAM REGION IX2
EEP-ROM 41
M1
M
NON-VOLATILE DATA REGION Dx
EEP-ROM 42
M2
WORK REGION RAM 2

FIG. 9


START
WRITE INSTRUCTION
S1
N ← 0
S2
N ← N+1
S3
PGM ← 1
S4
1ms COUNT
S5
PGM ← 0
S6
VERIFY
S7
≠
=
PGM ← 1
S8
3Nms COUNT
S9
PGM ← 0
S10
N = 25
S11
NO
YES
FAILURE
S12
END

Declaration and Power of Attorney For Patent Application

特許出願宣言書
Japanese Language Declaration

ATTORNEY'S DOCKET NO. (IF ANY)
HIT 2 010

私は、下欄に氏名を記載した発明者として、以下のとおり宣言する：

As a below named inventor, I hereby declare that:

私の住所、郵便の宛先および国籍は、下欄に氏名に続いて記載したとおりであり、

My residence, post office address and citizenship are as stated below next to my name,

名称の発明に関し、請求の範囲に記載した特許を求める主題の本来の、最初にして唯一の発明者である（一人の氏名のみが下欄に記載されている場合）か、もしくは本来の、最初にして共同の発明者である（複数の氏名が下欄に記載されている場合）と信じ、

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

_____

_____

_____

Microcomputer

_____

_____

その明細書を
（該当する方に印を付す）

☐ ここに添付する。

☐ _____ 日に出願番号

第 _____ 号として提出し、

_____ 日に補正した。
（該当する場合）

the specification of which

(check one)

☒ is attached hereto.

☐ was filed on _____ as

Application Serial No. _____

and was amended on _____
(if applicable)

私は、前記のとおり補正した請求の範囲を含む前記明細書の内容を検討し、理解したことを陳述する。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37部第1章第56条（a）項に従い、本願の審査に所要の情報を開示すべき義務を有することを認める。

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

Japanese Language Declaration

私は、合衆国法典第35部第119 条にもとづく下記の外国特許出願または発明者証出願の外国優先権利益を主張し、さらに優先権の主張に係わる基礎出願の出願日前の出願日を有する外国特許出願または発明者証出願を以下に明記する：

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior foreign applications
先の外国出願

(Number) (番 号)	(Country) (国 名)	(Day/Month/Year Filed) (出願の年月日)	Priority claimed 優先権の主張 Yes あり	No なし
61-65739	Japan	March 26, 1986	☒	☐
			☐	☐
			☐	☐

私は、合衆国法典第35部第120 条にもとづく下記の合衆国特許出願の利益を主張し、本願の請求の範囲各項に記載の主題が合衆国法典第35部第112 条第1項に規定の態様で先の合衆国出願に開示されていない限度において、先の出願の出願日と本願の国内出願日またはＰＣＴ国際出願日の間に公表された連邦規則法典第37部第1章第56条（a）項に記載の所要の情報を開示すべき義務を有することを認める：

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.) (出願番号)	(Filing Date) (出願日)	(現 況) (特許済み、係属中、放棄済み)	(Status) (patented, pending, abandoned)

私は、ここに自己の知識にもとづいて行った陳述がすべて真実であり、自己の有する情報および信ずるところに従って行った陳述が真実であると信じ、さらに故意に虚偽の陳述等を行った場合、合衆国法典第18部第1001条により、罰金もしくは禁錮に処せられるか、またはこれらの刑が併科され、またかかる故意による虚偽の陳述が本願ないし本願に対して付与される特許の有効性を損うことがあることを認識して、以上の陳述を行ったことを宣言する。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration

委任状：私は、下記発明者として、以下の代理人をここに選任し、本願の手続を遂行すること並びにこれに関する一切の行為を特許商標庁に対して行うことを委任する。
（代理人氏名および登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (*list name and registration number*)

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Daniel G. Blackhurst, Reg. No. 24,039
Robert E. Bushnell, Reg. No. 27,774
Christopher B. Fagan, Reg. No. 22,987
Robert J. Fay, Reg. No. 16,921
John X. Garred, Reg. No. 31,830
Jeffrey M. Ketchum, Reg. No. 31,174
Thomas E. Kocovsky, Jr., Reg. No. 28,383
James W. McKee, Reg. No. 26,482
Richard J. Minnich, Reg. No. 24,175
Jay F. Moldovanyi, Reg. No. 29,678
Patrick R. Roche, Reg. No. 29,580
Albert P. Sharpe, III, Reg. No. 19,879

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John X. Garred
Reg. No.31,830 (216) 861-5582

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発明者の署名・ 日付	SIGNATURE DATE Naoki Mitsuishi March 2, 1987
住所	RESIDENCE Hitachiseishinryo, 1503, Josui-hon-cho, Kodaira-shi, Tokyo, Japan
国籍	CITIZENSHIP Japanese
郵便住所	POST OFFICE ADDRESS Same as Residence
第二の共同発明者氏名	FULL NAME OF SECOND JOINT INVENTOR, IF ANY
発明者の署名 日付	SIGNATURE DATE
住所	RESIDENCE
国籍	CITIZENSHIP
郵便住所	POST OFFICE ADDRESS

第三の共同発明者氏名	FULL NAME OF THIRD JOINT INVENTOR, IF ANY
発明者の署名　　日付	SIGNATURE　　DATE
住所	RESIDENCE
国籍	CITIZENSHIP
郵便住所	POST OFFICE ADDRESS
第四の共同発明者氏名	FULL NAME OF FOURTH JOINT INVENTOR, IF ANY
発明者の署名　　日付	SIGNATURE　　DATE
住所	RESIDENCE
国籍	CITIZENSHIP
郵便住所	POST OFFICE ADDRESS
第五の共同発明者氏名	FULL NAME OF FIFTH JOINT INVENTOR, IF ANY
発明者の署名　　日付	SIGNATURE
住所	CITIZENSHIP
国籍	RESIDENCE
郵便住所	POST OFFICE ADDRESS